IN THE CLAIMS

Kindly amend claims 1, 6 and 8 as shown in the following claim listing of all claims:

1. (currently amended) Digital signal processing apparatus comprising a plurality of available hardware resource means and a first instruction set means having access to said available hardware resource means, so that at least a part of said hardware resource means execute operations under control of said first instruction set means;
characterized by a second instruction set means having access to only a predetermined limited subset of said plurality of available hardware resource means, so that at least a part of said predetermined limited subset of said hardware resource means execute operations under control of said second instruction set means, wherein in case of an interrupt the state of all of said limited subset of hardware resource means are stored within a single clock cycle and all hardware resource means under control of said first instruction set means have their state frozen.

2. (original) Apparatus according to claim 1, wherein said available hardware resource means are processor resource means.

3. (previously presented) Apparatus according to claim 1, comprising first state buffer means for storing the current state of hardware resource means in case of an interrupt, characterized in that in case of an interrupt said first state buffer means stores the current state of at least a part of such hardware resource means which are not included in said predetermined limited subset of said hardware resource means.

4. (original) Apparatus according to claim 3, characterized by second state buffer means for storing in case of an interrupt the current state of at least a part of said predetermined limited subset of said hardware resource means, said second state buffer means having a smaller size than that of said first state buffer means.

5. (original) Apparatus according to claim 4, comprising means for supplying power to said second state buffer means, characterized in that said power supply means essentially supplies power to said second state buffer means only during interrupt handling.

6. (currently amended) Apparatus according to claim 4, characterized in that at least a part of such hardware resource means which are not directly ~~accessable~~ accessible and not included in said predetermined limited subset of said hardware resource means are chained together in a first scan chain means and at least a part of such hardware resources which are not directly ~~accessable~~ accessible and included in said predetermined limited subset of said hardware resource means are chained together in a second scan chain means.

7. (previously presented) Apparatus according to claim 1, characterized in that said second instruction set means does not allow operations in parallel.

8. (currently amended) Method for processing digital signals in a digital signal processing apparatus comprising a plurality of available hardware resource means wherein at least a part of said hardware resource means execute operations under control of a first instruction set;
characterized in that at least a part of a predetermined limited subset of said plurality of available hardware resource means execute operations under control of a second instruction set having

access to only said predetermined limited subset of said hardware resource means, wherein in case of an interrupt the state of all of said limited subset of hardware resource means are stored within a single clock cycle and all hardware resource means under control of said first instruction set means have their state frozen.

9. (original) Method according to claim 8, wherein in case of an interrupt the current state of hardware resource means are stored in first state buffer means;
characterized in that in case of an interrupt the current state of at least a part of such hardware resource means which are not included in said predetermined limited subset of said hardware resource means are stored in said first state buffer means.

10. (original) Method according to claim 9,
characterized in that in case of an interrupt the current state of at least a part of said predetermined limited subset of said hardware resource means are stored in a second state buffer means having a smaller size than that of said first state buffer means.

11. (original) Method according to claim 10,
characterized is that power in essentially supplied to said second state buffer means only during interrupt handling.

12. (previously presented) Method according to claim 8, characterized in that said second instruction set does not allow operations in parallel.